

Thunder K8HM

///

S3892

Version 1.0

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#### Check the box contents!

The retail motherboard package should contain the following:



If any of these items are missing, please contact your vendor/dealer for replacement before continuing with the installation process.

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#### **Chapter 1: Introduction**

#### 1.1 - Congratulations

You have purchased one of the most powerful server solutions available. The Thunder K8HM (S3892) is a high-end server motherboard, based on the ServerWorks BCM5780 & BCM5785 chipsets. It also includes the NS PC87417 Super I/O and SMSC EMC6D 103S Hardware Monitoring chipsets.

This motherboard is designed to support up to two AMD Opteron ™ 200 Series processors and 16GB/32GB of DDR400/333 memory. The S3892 is ideal for CPU, memory, and network intensive applications required in the HPC and clustering environments.

Remember to visit TYAN's Website at <a href="http://www.tvan.com">http://www.tvan.com</a>. There you can find information on all of TYAN's products with FAQs, online manuals and BIOS uporades.

#### 1.2 - Hardware Specifications

#### Processor s

- Two uPGA 940 -pin ZIF sockets
   Supports up to two AMD Opteron™
   200 Series processors (inc luding dual core processors)
- Integrated 128-bit DDR memory controller

#### Chipse

- ServerWorks BCM5780 + BCM5785 chipsets
- National PC87417 Super I/O chip

#### Memory

- 128-bit dual channel memory bus • Total sixteen (16) 184-pin 2.5V DDR
- DIMM sockets (8 on CPU1 and 8 on CPU2)
- Supports PC1600/2100/2700
- Registered, ECC/Non-ECC module supported

## Expansion Slots

 Two (2) PCI Express X16 slots (each w/ x8 signal)

# Integrated Video Controller • ATI ES1000 controller

- 32MB DDR frame buffer
- 32MB DDR Hallie bulle

# Integrated Enhanced IDE Controller

- •Integrated Enhanced IDE Controller
- Single-channel master mode supports up to two IDE devices
- Supports IDE drives and ATAPIcompliant devices

#### Integrated SATA Controllers

- Supports four SATA-II ports at 3.0 Gb/s (BCM5785 Chipset)
- RAID 0/1/5 supported

#### Integrated LAN Controllers

- Dual GbE LAN (from BCM 5780)
   Embedded in BCM5780
- Embedded in BCM5780
   Two 10/100/1000 RJ-45 LAN ports
- w/LED
   One Intel i82551 QM fast Ethernet
- controller
- One 10/100 RJ-45 LAN port w/LED

- Two (2) PCI X 133/100MHz slots
- One (1) PCI-X 100MHz slot
- One (1) PCI 32-bit/33MHz, v2.3 compliant slot
- One (1) TYAN "TARO " SO-DIMM socket

#### System Management

- Two (2) EMC6D103S hardware monitoring IC
- Eight (8) 3+1 fan headers support
- tachometer monitoring, six (6) of them with smart FAN control • Temperature and voltage monitoring
- Watchdog timer support

## Integrated I/O

- One floppy connector
- One IDE connector
- Four SATA connectors
- Four USB2.0 ports (2 at rear, 2 via cable)
- Two COM ports (1 at rear, 1 via cable)
- Tyan 2 x 9 front panel pin header
- Tyan 2 x 6 front panel pin header for LAN/ID LED
- 2 x 25 connector for optional TYAN IPMI SMDC

#### Back Panel I/O Ports

- · Stacked PS/2 Mouse & Keyboard ports
- Stacked 2 USB ports and 1 10/100 RJ45 port
- One 9-pin COM port
   One 15-pin VGA connector
- Two side-by-side RJ-45 ports

#### Form Factor

- Extended ATX footprint (13" x 12")
- EPS12V/SSI v3.51 (24+8) power connectors

- Operating on 32bit/33MHz PCI bus

#### **Optional Modules**

- M3291, IPMI 2.0 Remote System Mgmt card
- Renesas H8S2167 BMC controller
   BT, KCS, Log ging support

- IPMI-over-LAN - Remote power on/off and reset
- M7901/M7902, Ultra 320 SCSI TARO
- Adaptec AIC-7901/7902 single/dual-channel Ultra 320 SCSI controller
- Adaptec Host RAID 0, 1, 10 supported
- M9000 SAS/SATA II TARO card - Adaptec AIC-9405/9410 SAS controller
- Supports up to 4-port (M9000-5) and 8-port (M9000-10) SAS & SATA running
- at 3.0Gb/s - Adaptec HostRAID 0, 1 & 10 supported

#### BIOS

- AMI BIOS on 8Mbit LPC Flash ROM
- · Serial Console Redirect
- PXE via Ethernet, USB device boot
   SMBIOS 2.3.1. BBS 1.1 compliant
- Headless Operation via serial console redirect
- 48-bit LBA Support

#### Power

- Onboard dual 4-phase VRM
- EPS12V/SSI v3.51 (24+8) power

#### Regulatory

• FCC Class B (DoC), CE (DoC)

#### **Chapter 2: Board Installation**

Precautions: The Thunder K8HM supports SSI, EPS12V type power supplies (24pin + 8pin) and will not operate with any other types. For proper power supply installation procedures see page 37.

**DO NOT USE** ATX 2.x or ATXGES power supplies as they will damage the board and void your warranty.

How to install our products right... the first time

The first thing you should do is reading this user's manual. It contains important information that will make configuration and setup much easier. Here are some precautions you should take when installing your motherboard:

- (1) Ground yourself properly before removing your motherboard from the antistatic bag. Unplug the power from your computer power supply and then touch a safely grounded object to release static charge (i.e. power supply case). For the safest conditions, TYAN recommends wearing a static safety wrist strap.
- (2) Hold the motherboard by its edges and do not touch the bottom of the board, or flex the board in any way.
- (3) Avoid touching the motherboard components, IC chips, connectors, memory modules, and leads.
- (4) Place the motherboard on a grounded antistatic surface or on the antistatic bag that the board was shipped in.
- (5) Inspect the board for damage.

The following pages include details on how to install your motherboard into your chassis, as well as installing the processor, memory, disk drives and cables.

NOTE

DO NOT APPLY POWER TO THE BOARD IF IT HAS BEEN

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#### 2.1- Board Image

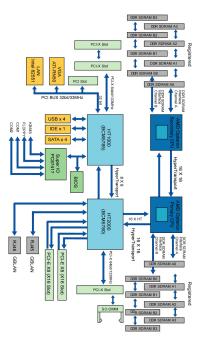
This picture is representative of the latest board revision available at the time of publishing. The board you receive may or may not look exactly like the above picture.



The following page includes details on the vital components of this

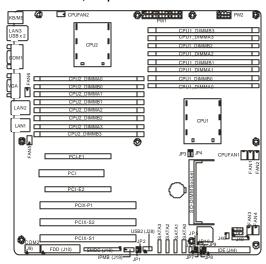
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# 2.2 - Block Diagram



Thunder K8HM (S3892) Block Diagram

# 2.3 - Board Parts, Jumpers and Connectors



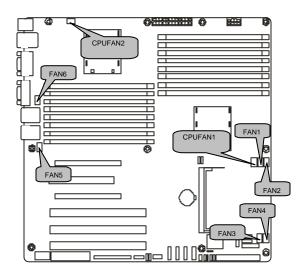
This diagram is representative of the latest board revision available at the time of publishing. The board you receive may not look exactly like the above diagram.

#### Jumper Legend

Γ	OPEN - Jumper OFF, without jumper cover
Г	CLOSED – Jumper ON, with jumper cover

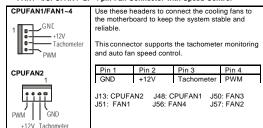
10

Jumper/Connector	Function
FAN5/FAN6	4-pin Fan Connector
CPUFAN1/CPUFAN2/FAN1/ FAN2/FAN3/FAN4	4-pin Fan Connector with Speed Control
J19	IPMB Connector
J28	USB Front Panel Connector
J30/J39/J40/J41	SATA Connectors
J47	LAN & ID LED and ID Switch Connector
J49	Front Panel Header
JP1/JP2	SMDC/ASF2.0 Select Jumper (Close 1-2) Default, support ASF 2.0 (Close 2-3) support SMDC card
JP3	VGA Enable/Disable Jumper (Close 1-2) Default, enabled (Close 2-3) Disabled
JP4	LAN3 Enable/Disable Jumper (Close 1-2) Default, enabled (Close 2-3) Disabled
JP5/JP8	PCI-X Mode Select Jumper (Close 1-2) Default, Based on Card (Close 2-3) Force to run at PCI mode (only 66 or 33 MHz)
JP7/JP9	PCI-X Frequency Select Jumper (Close 1-2) Default, based on Card (Close 2-3) 100MHz or less
JP10	Clear CMOS Jumper (Close 1-2) Default (Close 2-3) Clear CMOS
J43/J46/J60	Reserved for OEM only

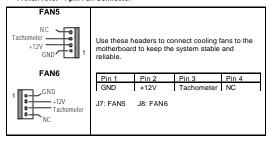


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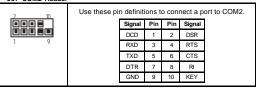
#### FAN1~4/CPUFAN1~2: 4-pin Fan Connector with Speed Control



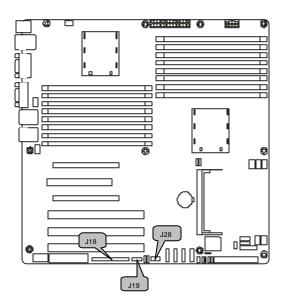
#### FAN5/FAN6: 4-pin Fan Connector



#### J9: COM2 Header



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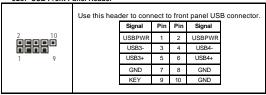
14 http://www.tyan.com

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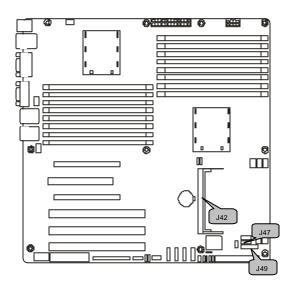
#### J19: IPMB Pin Header

Pin 1 IPMB Pin 2 GNE DATA Pin 3 IPMB Pin 4 NC					
		Pin 1		Pin 2	GND
Pin 3 IPMB Pin 4 NC	100001		DATA		
	$\underbrace{}_{1}$	Pin 3	IPMB	Pin 4	NC
CLK	1		CLK		

#### J28: USB Front Panel Header



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#### J42: SO-DIMM Socket



#### J47: LAN & ID LED and ID Switch Connector



Use these pin definitions to connect a port to LAN & ID LED and ID Switch.

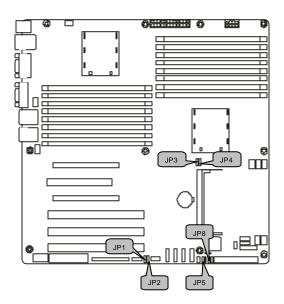
Signal	Pin	Pin	Signal
LAN1 LED+	1	2	LAN1 LED-
LAN2 LED+	3	4	LAN2 LED-
LAN3 LED+	5	6	LAN3 LED-
ID LED+	7	8	ID LED1-
ID S/W+	9	10	ID S/W-
NC	11	12	KEY

#### J49: Front Panel Header

SMBUS Data	6VSB	Non-mask	Interupt (NMI)	RESET	Switch	HDD LED-	HDD LED+
5	<b>a</b>	11	9	7	ω ω	ω	1
16	14	12	9	8	6	4	2
GND	Key	Warning LED-	Waming LED+	POWER	Switch	PWR LED-	PWR LED+
	15	15 13 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	15 13 11 10 11 11 12	15 13 11 9	15 13 11 0 7 10 10 10 10 10 10 10 10 10 10 10 10 10 1	15 13 11 0 7 6 10 10 10 10 10 10 10 10 10 10 10 10 10 1	

The motherboard provides one front panel header for electrical connection to the front panel switches and LED's.

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http://www.tyan.com

#### JP1/JP2: SMDC/ASF2.0 Select Jumper

JP1 JP2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	(Default) - Support ASF2.0
JP1 JP2 1 II 1 II II II II	Support SMDC card

#### JP3: VGA Enable/Disable Jumper

1	(Default) - Enable VGA
1 🗓	Disable VGA

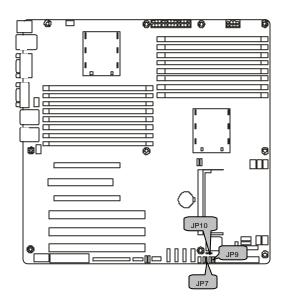
#### JP4: LAN3 Enable/Disable Jumper

1 3	(Default) - Enable LAN3 (Intel 82551)
1 1 3	Disable LAN3

#### JP5/JP8: PCI-X Mode Select Jumper

3 🔳	(Default) - Based on card
3 <b>□</b> 1 <b>□</b>	Force to run at PCI mode (only 66 or 33 MHz)

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http://www.tyan.com

#### JP7/JP9: PCI-X Frequency Select Jumper

3 0 1	(Default) - Based on card
3	Force to run at 100MHz or less

#### JP10: Clear CMOS Jumper

3 <b>II</b>	If you have lost your system/setup password or need to clear the system BIOS settings. You can reset the CMOS settings by using this jumper.
(Clear) 3 1 1 (Default)	Power off the system and set JP10 to (2-3) position, and then power on to boot up the system. The CMOS will be cleared when the screen is on. Finally shut down the power, replace JP10 to the default setting (1-2), power on the system again after done.

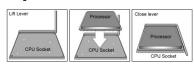
#### 2.4 - Installing the Processor(s)

Your brand new Thunder K8HM supports the latest 64-bit processor technology from AMD. Only the AMD Opteron processor 200 series are certified and supported with this motherboard. Check our website for latest processor support. <a href="http://www.tvan.com">http://www.tvan.com</a>



If using a single processor, it MUST be installed in socket CPU1. When using a single processor only CPU1 memory banks are addressable.

TYAN is not liable for damage as a result of operating an unsupported configuration.



The diagram is provided as a visual guide to help you install socket processors and may not be an exact representation of the processors you have.

Step 1: Lift the lever on the socket until it is approximately 90  $^{\circ}$  or as far back as possible to the socket.

Step 2: Align the processor with the socke t. There are keyed pins underneath the processor to ensure that the processor's installed correctly.

Step 3: Seat the processor firmly into the socket by gently pressing down until the processor sits flush with the socket.

Step 4: Place the socket lever back down until it locks into place. The installation is finished.

Repeat these steps for the second processor if you are using two processors.

Take care when installing processors as they have very fragile connector pins below the processor and can bend and break if inserted improperly.

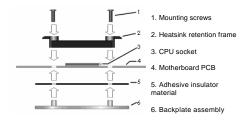
#### 2.5 - Heatsink Retention Frame Installation

After you are done installing the processor(s), you should proceed with installing the retention frame and heatsink. The CPU heatsink will ensure that the processors do not overheat and continue to operate at maximum performance for as long as you own them. Overheated processors are dangerous to the motherboard.

The backplate assembly prevents excessive motherboard flexing in the area near the processor and provides a base for the installation of the heatsink retention bracket and heatsink.

Because there are many different types of heatsinks available from many different manufacturers, a lot of them have their own method of installation. For the safest method of install ation and information on choosing the appropriate heatsink, use heatsinks validated by AMD. Please refer to AMD's website at <a href="https://www.amd.com">www.amd.com</a>.

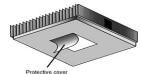
The following diagram will illustrate how to install the most common CPU back plates:



NOTE: Please see next section for specific instructions on how to install mounting bracket.

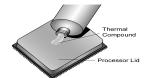
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#### 2.6 - Thermal Interface Material



There are two types of thermal interface materials designed for use with the AMD Opteron processor.

The most common material comes as a small pad attached to the heatsink at the time of purchase. There should be a protective cover over the material. Take care not to touch this material. Simply remove the protective cover and place the heatsink on the processor.



The second type of interface material is usually packaged separately. It is commonly referred to as 'thermal compound'. Simply apply a thin layer on to the CPU lid (applying too much will actually reduce the cooling).



Always check with the manufacturer of the heatsink & processor to ensure the Thermal Interface material is compatible with the processor & meets the manufacturer's warranty requirements

#### 2.7 - Heatsink Installation Procedures

#### Type A: CAM LEVER (TYPE) INSTALLATION



After placing backplate and interface material under motherboard place heatishk retention frame on top of motherboard. Align plastic retention bracket screw holes with CPU backplate standoffs.

Tighten screws to secure plastic retention bracket. Repeat for the other side. DO NOT OVER TIGHTEN.



2. After tightening screws secure metal clip to plastic retention bracket center tab. Repeat for the other side of heatsink.



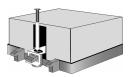
3. After securing metal clip to plastic retention bracket center tab, push down on plastic clip to lock plastic clip to side tab.

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#### Type B: SCREW RETENTION TY PE HEATSINK



After placing CPU back-plate and adhesive interface material under motherboard, place heatsink retention frame on top of motherboard. Align heatsink retention frame screw hole with backplate assembly standoffs. Place heatsink inside plastic retention bracket. Place metal clip over retention frame tab. Repeat for other side.



2. Insert screw through metal clip. BE SURE METAL CLIP IS LOCKED ONTO RETENTION FRAME TAB.



3. Tighten screw through metal clip. Repeat on the other side. **DO NOT OVER TIGHTEN.** 

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#### Finishing Installing the Heatsink

After you have finished installing the heatsink onto the processor and socket, attach the end wire of the fan (which should already be attached to the heatsink) to the motherboard. The following diagram illustrates how to connect fans onto the motherboard.



Once you have finished installing all the fans you can connect your drives (hard drives, CD-ROM drives, etc.) to your motherboard.

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#### 2.8 - Tips on Installing Motherboard in Chassis

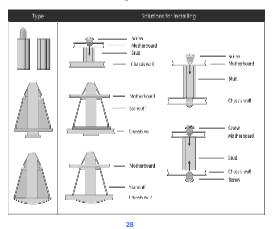
Before installing your motherboard, make sure your chassis has the necessary motherboard support studs installed. These studs are usually metal and are gold in color. Usually, the chassis manufacturer will pre-install the support studs. If you are unsure of stud placement, simply lay the motherboard inside the chassis and align the screw holes of the motherboard to the studs inside the case. If there are any studs missing, you will know right away since the motherboard will not be able to be securely installed.

Pay attention when installing board in chassis. Some components are near the mounting holes and can be damaged.

Some chassis' include plastic studs instead of metal. Although the plastic studs are usable, TYA N recommends using metal studs with screws that will fasten the motherboard more securely in place.

Below is a chart detailing what the most common motherboard studs look like and how they should be installed.

Mounting the Matheband



#### 2.9 - Installing the Memory

Before attempting to install any memory, make sure that the memory you have is compatible with the motherboard as well as the processor. The following diagram shows common types of DDR SDRAM modules:



#### Key points to note before installing memory into Thunder K8HMt

For optimal dual-channel DDR operation, always install memory in pairs beginning with CPU1\_DIMMA3 and CPU1\_DIMMB3. Memory modules of the same type and density are required for dual-channel DDR operation. Mismatched memory may cause system instability.

Refer to the following table for supported DDR populations . (Note: X indicates a populated DIMM slot)

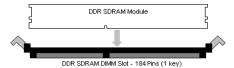
	Single CPU Installed (CPU1_only)			Dual CPU installed (CPU1 and CPU2)				
Population Option	1	2	3	4	5	6	7	8
CPU1 DIMMA0				х				×
CPU1_DIMMB0				Х				Х
CPU1_DIMMA1			х	Х			Х	х
CPU1_DIMMB1			х	Х			х	х
CPU1_DIMMA2		Х	Х	Х		х	х	Х
CPU1 DIMMB2		×	×	х		х	х	×
CPU1_DIMMA3	Х	х	Х	Х	х	Х	х	Х
CPU1_DIMMB3	Х	х	х	Х	х	Х	Х	х
CPU2_DIMMA0								Х
CPU2_DIMMB0								Х
CPU2_DIMMA1							х	х
CPU2 DIMMB1							х	×
CPU2_DIMMA2						Х	х	Х
CPU2_DIMMB2						х	х	х
CPU2_DIMMA3					Х	х	х	Х
CPU2 DIMMR3					v	v	v	v

When the DIMMs are not fully populated, the system can support 1 28MB, 256MB, 512MB, 1GB and 2GB of PC2100/2700 Registered memory modules.

However, if 8 DIMMs and 16 DIMMs are populated for single and dual CPU operation respectively, the system can only support up to PC2100. All installed memory will be automatically detected. The T hunder K8HM S3892 supports up to 32GB of memory.

#### **Memory Installation Procedure**

When you install the memory modules, make sure the module aligns properly with the memory slot. The modules are keyed to ensure that it is inserted only one way. The method of installing memory modules are detailed by the following diagrams.



Once the memory modules are firmly seated in the slot, two latches on either side will close and secure the module into the slot. Sometimes you may need to close the latches yourself.



To remove the memory module, simply push the latches outwards until the memory module pops up. Then remove the module.



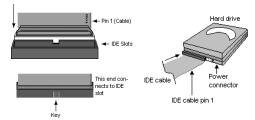
YOU MUST ALWAYS unplug the power connector from the motherboard before performing system hardware changes. Otherwise you may damage the board and/or expansion device.

#### 2.10 - Attaching Drive Cables

#### Attaching IDE Drive Cable

Attaching the IDE drive cable is simple. The cable is "keyed" to only allow it to be connected in the correct manner.

Attaching IDE cable to the IDE connector is illustrated below:



Simply plug in the BLUE END of the IDE cable into the motherboard IDE connector, and the other end into the drive. Each standard IDE cable has three connectors, two of which are closer together. The BLUE connector that is furthest away from the other two is the end that connects to the motherboard. The other two connectors are used to connect to drives.

Note: Always remember to properly set the drive jumpers. If only using one device on a channel, it must be set as Master for the BIOS to detect it.

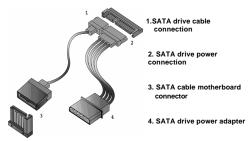
# TIP: Pin 1 on the IDE cable (usually designated by a colored wire) faces the drive's power connector.

#### Attaching Serial ATA Cables

The Thunder K8HM is also equipped with 4 Serial ATA (SATA) channels. Connections for these drives are also very simple.

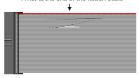
There is no need to set Master/Slave jumpers on SATA drives.

#### The following pictures illustrate how to connect an SATA drive



Attaching Floppy Drive Cables
Attaching floppy diskette drives are done in a similar manner to hard drives. See the picture below for an example of a floppy cable. Most of the current floppy drives on the market require that the cable be installed with the colored stripe positioned next to the power connector. In most cases, there will be a key pin on the cable which will force a proper connection of the cable.

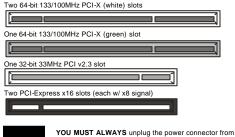
Twist at the end of the ribbon cable



Attach first floppy drive (drive A:) to the end of the cable with the twist in it. Drive B: is usually connected to the next possible connector on the cable (the second or third connector after you install Drive A:).

#### 2.11 - Installing Add-In Cards

Before installing add-in cards, it's helpful to know if they are fully compatible with your motherboard. For this reason, we've provided the diagrams below, showing the most common slots that may appear on your motherboard. Not all of the slots shown will necessarily appear on your motherboard.



NOTE the motherboard before performing system hardware changes. Otherwise you may damage the board and/or expansion device.

Simply find the appropriate slot for your add-in card and insert the card firmly. Do not force any add-in cards into any slots if they do not seat in place. It is better to try another slot or return the faulty card rather than damaging both the motherboard and the add-in card.

#### 2.12 - Installing Optional SO-DIMM Modules

Your Thunder K8HM S3892 motherboard is equipped with an optional propri etary SO-DIMM connector. The SO-DIMM connector can be used for expansion cards to provide such features as, additional SAS/SATA II or SCSI support. For details of available expansions cards, visit the TYAN website at <a href="http://www.tvan.com">http://www.tvan.com</a>. To install a SO-DIMM expansion cards.

1. Open the spring levers as shown.



- Insert the SO-DIMM card as shown, making sure that the card is the right way up. The card will fit in only one way and the screw holes in the card should line up exactly with the mounting posts on the motherhoard
- Push the SO-DIMM card down into place and make sure the spring levers click into place as shown



 Screw the board into place using one or two screws as required.

Removal of a SO-DIMM card is a reversal of the install ation procedure. Push out the spring levers as shown and pull the card out of the socket.





The SO-DIMM expansion cards will fit in the slot only one way. Make sure that you align the slot in the card with the key in the c ard slot.

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#### 2.13 - Connecting External Devices

Your motherboard supports a number of different interfaces for connecting peripherals. Some I/O ports may not be available with the board due to the different configurations.

#### PS/2 Mouse/Keyboard



Peripheral devices can be plugged straight into any of these ports but sof tware may be required to complete the installation.

LAN1 and LAN2 LED Color Definition
The two onboard LAN ports have green LEDs to indicate the LAN status. The chart below illustrates the different LED states.

	LAN1 and LAN2 Link/Activiev LED Scheme					
Left Right	Left LED	Right LED				
	Activity	Link				
	Green (Blink)	Green				

#### LAN3 LED Color Definition

The onboard Ethernet port has green and yellow LEDs to indicate LAN status. The chart below illustrates the different LED states.

	10/100 Mbps LAN3 Link/Activity LED Scheme			
	Speed	Left LED	Right LED	
	Link 10Mbps	Green	Off	
Left Right	Activity 10Mbps	Green (Blink)	Off	
	Link 100Mbps	Green	Green	
	Activity 100Mbps	Green (Blink)	Green	

# 2.14-Installing the Power Supply

There are two power connectors on your Thunder K8HM.

The Thunder K8HM requires an EPS12V (24 pin + 8 pin) power supply to boot.

Please be aware that ATX 2.x and ATXGES power supplies are  $\underline{\text{not}}$   $\underline{\text{compatible}}$  with the board and can damage the motherboard and/or CPU(s).

#### EPS12V Main Power 24-Pin (Chipsets & Components)

1	12
	H
13	24

12	+3.3V	24	GND
11	+12V2	23	+5V
10	+12V2	22	+5V
9	+5VSB	21	+5V
8	PWROK	20	RESVD
7	GND	19	GND
6	+5V	18	GND
5	GND	17	GND
4	+5V	16	PSON#
3	GND	15	GND
2	+3.3V	14	-12V
1	+3.3V	13	+3.3V



EPS 12V 8-pin (CPU Power)					
4	GND	8	+12V3		
3	GND	7	+12V3		
2	GND	6	+12V3		
1	GND	5	+12V3		

Applying power to the board

- Connect the EPS 12V 8-pin power connector.
- Connect the EPS 12V 24-pin power connector.
  Connect power cable to power supply and power outlet



YOU MUSTunplug the power supply from the wall outlet before plugging the power cables to motherboard connectors.

# 2.14 - Finishing Up

Congratulations! You're finished setting up the hardware as pect of your computer. Before closing up your chassis, make sure that all cables and wires are connected properly, especially IDE cables and jumpers. You may have difficulty powering on your system if the motherboard jumpers are not

In the rare circumstance that you have experienced difficulty, you can find help by asking your vendor for assistance. If they are not available for assistance, please find setup information and documentation online at our website or by calling your vendor's support line.

# **Chapter 3: BIOS**

#### 3.1 - BIOS Setup Utility

With the BIOS setup utility, you can modify BIOS settings and control the special features of your computer. The setup utility uses a number of menus for making changes and turning the special features on or off.

NOTE

All menus are based on a typical system. The actual menus displayed on your screen may be different and depend on the hardware and features installed in your computer.

- To start the BIOS setup utility:
  a. Turn on or reboot your system
  - Press <Del> during POST (F4 on remote console) to start BIOS setup utility

		BIOS Se	etup Utili	ty		
Mai	n Advanced	PCI/PnP	Boot	Security	Chinset	Fxit
System C	verview				Use [ENTE or [SHIFT-	
AMIBIOS					select a fie	ld
Version	: 08.00. xx					
Build Date	e: 08/31/05				Use [+] or	[-] to
ID	: 0AAAA000				configure s	system time.
Processor						
Type	: AMD Opteron	(tm) Model xxx				
Speed	: xxxx MHz					
Count	: x				? ? Sele	ct Screen
					? ? Selec	t Item
System M	lemory				+/- Char	ge Option
Size	: xxxx MB				F1 Gene	eral Help
					F10 Save	
System T		[22:21:21]			ESC Exit	
System Da	ate	[ Tue 01/01/2	002]			

#### To select an item

Use the left/right (  $\leftarrow$   $\rightarrow$ ) arrow keys to make a selection.

To display a sub-menu (A pointer " ▶ " marks all sub menus)

Use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>.

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## 3.2 - BIOS Menu Bar

The menu bar at the top of the windows lists these selections:

Main	To configure basic system setups
Advanced	To configure the advanced chinset features
PCI/PnP	To configure legacy Plug & Play or PCI settings
Boot	To configure system boot order
Security	To configure user and supervisor passwords
Chipset	To configure chipset management features
Evit	To exit setup utility

NOTE Options written in **bold type** represent the BIOS setup default

## 3.3 - BIOS Legend Bar

The chart describes the legend keys and their alternates:

Kev	Function		
<f1></f1>	General help window		
<esc></esc>	Exit current menu		
← → arrow kevs	Select a different menu		
↑ or ↓ arrow keys	Move cursor up/down		
<tab> or <shift-tab></shift-tab></tab>	Cycle cursor up/down		
<home> or <end></end></home>	Move cursor to top/bottom of the window		
<pgup> or <pgdn></pgdn></pgup>	Move cursor to next/previous page		
<->	Select the previous value/setting of the field		
<+>	Select the next value/setting of the field		
<f8></f8>	Load Fail Safe default configuration values of the menu		
<f9></f9>	Load the Optimal default configuration values of the		
	menu		
<f10></f10>	Save and exit		
<enter></enter>	Execute command or select submanu		

## 3.4 - BIOS Main Menu

The Main BIOS Menu is the first screen that you can navigate. The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed -out" options cannot be configured, options in blue can be changed.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often, a text message will accompany it.

BIOS Setup Utility		
Main Advanced PCI/PnP Boot Security	Chipset Exit	
System Overview	Use [ENTER], [TAB] or [SHIFT-TAB] to select a	
	field	
AMIBIOS		
Version : 08.00.xx	Use [+] or [-] to	
Build Date: 08/31/05	configure system time.	
ID : 0AAAA000		
Processor		
Type : AMD Opteron(tm) Model xxxx		
Speed : xxxx MHz		
Count : x	? ? Select Screen	
	? ? Select Item	
System Memory	Enter Go to Sub Screen	
Size : xxxx MB	F1 General Help	
	F10 Save and Exit	
System Time [22:21: 21]	ESC Exit	
System Date [ Tue 01/01/2002]		

Feature	Option	Description
Main		
System Time	HH: MM: SS	Set the system time
Custom Date	MM - DD - VVVV	Cat the austom data

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## 3.5 - BIOS Advanced Menu

You can select any of the items in the left frame of the screen, such as Super I/O Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <a href="Arrows keys. All">Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.

BIOS Setup Utility Main Advanced PCI/PnP Boot Secur	ity Chipset Exit
Advanced Settings	
WARING: Setting wrong values in below sections may cause system to malfunction.  > CPU Configuration  > IDE Configuration  > Super IO Configuration  > SATA Configuration  > ACPI Configuration  > Forth Configuration  > Event Log Configuration  > Hyper Transport Configuration  > Hyper Transport Configuration  > MPS Configuration  > MPS Configuration  > MPD Configuration  > MPD Configuration  > MD PowerNow Configuration  > AMD PowerNow Configuration  > Legis Secsion Configuration  > Legis Secsion Configuration  > Legis Configuration  > Legis Configuration  > Legis Configuration  > Legis Configuration  > Device & PCI Slots Configuration	Options for CPU  ? ? Select Screen ? ? Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit

Feature	Option	Description
Advanced Settings		
CPU Configuration	Menu Item	Options for CPU
IDF Configuration	Menu Item	Configure the IDF device(s)
Floppy Configuration	Manu Itam	Configure the Floppy drive(s)
Super IO Configuration	Menu Item	Configures Super IO Chipset
S-ATA Configuration	Menu Item	Configure ServerWorks
ACPI Configuration	Menu Item	Section for Advanced ACPI
Event Log Configuration	Menu Item	Mark as read, Clear or View Event Log statistics
Hyper Transport Configuration	Menu Item	Configure HT links
Hardware Health	Menu Item	Configure/monitor the

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Feature	Option	Description	
Advanced Settings			
MPS Configuration	Menu Item	Configure the Multi-Processor Table	
PCI Express Configuration	Menu Item	Configure PCI Express L0 and L1 link power states	
AMD PowerNow Configuration	Menu Item	Configure AMD PowerNow support	
Remote Access Configuration	Menu Item	Configure Remote Access	
USB Configuration	Menu Item	Configure the USB support	
Device & PCI Slots	Menu Item	Onboard Devices and PCI Add-	

## 3.5.1 CPU Configuration Sub-Menu

You can use this screen to view CPU Configuration Menu. Use the up and down arrow  $(\uparrow \land \downarrow)$  keys to select an item. Use the Plus and Minus  $(\star \land)$  keys to change the value of the selected option. The settings are described on the following pages.

	BIOS	Setup Uti	ility	
Main Advanced	PCI/PnP	Root	Security	Chipset Exit
CPU Configuration				This option should remain disabled for
Module Version : XX.XX Physical Count : X Logical Count : X				normal operation. The driver developer may disable it for testing purpose.
Dual Core AMD Opteron (tr Revision: XX Cache L1: XXXKB Cache L2: XXXXKB Speed: XXXXMHz Current FSB Multiplier: Maximum FSB Multiplier: Able to change Freq. : UCode Patch Level :	XXX XXX Yes	· xxx		? ? Select Screen ? ? Select Item +/- Change Option F1 General Help
GART Error Reporting MTRR Mapping	[Disabled] [Continuous	<b>6</b> ]		F10 Save and Exit ESC Exit

Feature	Option	Description
CPU Configuration		
Module Version Physical Count Logical Count	Read only	Displays information about CPU
Revision		
Cache L1		
Cache L2		
Speed	Deed sets	Disabase information about OBU
Current FSB Multiplier	Read only	Displays information about CPU
Maximum FSB Multiplier		
Able to change Freq.		
uCode Patch Level		

Feature	Option	Description
CPU Configuration		
GART Error Reporting	Disabled	This option should remain disabled for normal operation. The driver
GART Error Reporting	Enabled	developer may enable it for the purpose of testing.
MTRR Mapping	Continuous	This option determines the method used for programming CPU MTRRs when 4GB or more of memory is preset. Discrete leaves
м том маррину	Discrete	the PCI hole below the 4GB boundary undescribed. Continuous explicitly describes the

## 3.5.2- IDE Configuration Sub-Menu

You can use this screen to select options for the IDE Configuration Settings.
Use the up and down <a href="Arrow-keys">Arrow-keys</a> to select an item. Use the <a href="Plus">Plus</a> and <a href="Aminus">Aminus</a> keys to change the value of the selected option.

BIOS Setup Utility							
Main Advanced	PCI/PnP	Boot	Security	Chipset	Exit		
IDE Configuration				While enteri BIOS auto d			
Primary IDE Master Primary IDE Slave		[xxxx]		This displays auto detection	IDE devices. s the status of on of IDE		
IDE Detect Time Out (Sec) :		[xx]		devices.	Screen		
				? ? Select			
					e Option al Help and Exit		
				ESC Exit			

Feature	Option	Description						
IDE Configuration								
Primary IDE Master/Slave	Auto XXXX  Not Detected  Enabled	While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto detection of IDE devices.						
IDE Detect Time Out (Sec)	0~35 (at 5 interval)	Selects the time out value for detecting ATA/ATAPI device(s).						

## 3.5.2.1 - Primary/Secondary IDE Master/Slave Sub-Menu

	BIOS	Setup Utility		
Main Advanced Primary IDE Master	PCI/PnP	Boot S	ecurity Ch	ioset Exit
Device: Not Detected				Select Screen Select Item Change Option
Type LBA /Large Mode Block (Multi-Sector Transf er) PIO Mode DMA Mode S.M.A.R.T. 32 Bit Data Transfer		[Auto] [Auto] [Auto] [Auto] [Auto] [Auto] [Auto] [Enabled	Tab F1 F10 ESC	Select Field General Help Save and Exit

Feature	Option	Description
Configure Nat417 Super IO C	hipset	
Туре	Not Installed CD/DVD ARMD	Selects the type of device connected to the system.
LBA/Large Mode	Auto Disabled	Auto: Enabled LBA Mode if the device supports it and the device is not already formatted with LBA Mode disabled.
		Disabled: Disabled LBA Mode.
Block (Multi-Sector Transfer)	Auto	Disabled: The Data transfer from and to the device occurs one sector at a time.
Block (Walli-Sector Transfer)	Disabled	Auto: The Data transfer from and to the device occurs multiple sectors at a time if the device supports it
818.14	Auto	Selects the PIO Mode. Select Auto
PIO Mode	0~4 (at 1 interval)	to enhance hard disk performance by optimizing the hard disk timing.
DMA Mode	Auto	Selects DMA Mode. Auto: Auto detected.
	Auto	S.M.A.R.T (Self -Monitoring Analysis
S.M.A.R.T.	Disabled	and Reporting Technology) is a utility that monitors your disk status
	Enabled	to predict hard disk failure.
32Bit Data Transfer	Enabled	Enables 32-bit to maximize the IDE hard disk data transfer rate.

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## 3.5.3 - Floppy Configuration Sub-Menu

You can use this screen to specify options for the Floppy Configuration Settings. Use the up and down <arrow- keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option. The settings are described on the following pages.

	BIOS Setup Utility							
Main	Advanced	PCI/PnP	Root	Security	Chipset	Fxit		
Floppy Configuration					Select the type of floppy drive connected			
					to the syste	5111.		
Floppy A		[1.44 MB						
Floppy B		[Disabled]	l					
					? ? Sele	ct Screen		
					? ? Selec	t Item		
					+/- Chang	ge Option eral Help		
					F10 Save ESC Exit			

Feature	Ontion	Description
Floppy Configuration		
	Disabled	
Floppy A Floppy B	360 KB 51/4"	Selects the type of floppy drive
	1.2 MB 51/4"	connected to the system.
	720 KB 31/2"	
	1.44 MB 31/2'	
	2.88 MB 31/2"	

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## 3.5.4 - Super IO Configuration Sub-Menu

You can use this screen to select options for the Super I/O settings. Use the up and down arrow  $(\uparrow \land \lor)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option

Main Advanced	BIOS S PCI/PnP	Setup Utilit Boot	y Security	Chipset Exit
Configure Nat417 Super IO	Allows BIOS to enable or disable Floppy			
Onboard Floppy Controller Serial Port1 Address Serial Port2 Address		[Enable [3F8/IR [2F8/IR	Q4]	? ? Select Screen ? ? Select Item +/- Change Option F1 General Help F10 Save and Exit ESC Exit

Feature	Option	Description					
Configure Nat417 Super IO Chipset							
Onboard Floppy Controller	Enabled Disabled	Allows BIOS to enable or disable the floppy controller.					
	3E8/IRQ4	Allows BIOS to select Serial Port1					
Serial Port1 Address	2E8/IRQ3 Disabled	Base Addresses.					
Serial Port2 Address	2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Allows BIOS to select Serial Part2 Base Addresses.					
Serial Port2 Address	0_0/						

## 3.5.5 S-ATAConfiguration Sub-Menu

You can use this screen to view S-ATA Configuration Menu. Use the up and down arrow ( $\uparrow$ / $\downarrow$ ) keys to select an item. Use the Plus and Minus ( $_{+/}$ ) keys to change the value of the selected option. The settings are described on the following pages.

BIOS Setup Utility							
Main Advanced Configure ServerWorks	PCI/PnP	Root	Security	Chipset Exit  Enable HT1000 S-ATA.			
HT1000 S-ATA S-ATA Mode INT13 Support		[Enabled] [P-ATA] [Enabled]		? ? Select Screen ? ? Select Item +/- Change Option F1 General Help F10 Save and Exit ESC Exit			

Feature	Option	Description	
Configure ServerWorks			
LIT4000 O A T A	Enabled	Allows user to enable or disable	
HT1000 S-ATA	Disabled	HT1000 S-ATA controller.	
S-ATA Mode	P-ATA	Sets S-ATA mode as P-ATA	
3-ATA Wode	S-ATA	emulation or native S -ATA.	
INIT42 Cupped	Enabled	Faching or disching INIT42 cupper	
INT13 Support	Disabled	Enables or disa bles INT13 support.	

## 3.5.6 -ACPI Configuration Sub-Menu

Use this screen to select options for ACPI. Use the up and down arrow  $(\uparrow \land \lor)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on this page. The screen is shown helpow

Main <b>Advanced</b>	BIOS PCI/PnP	Setup Utility Boot	/ Security	Chipset	Exit
Main Advanced Advanced ACPI Configurat  ACPI Version Features ACPI APIC Support ACPI SRAT Table AMI OEMB table Headless mode		[ACPI v2.0] [Enabled] [Enabled] [Enabled] [Disabled]	Security	Enable RSD to 64-bit Fixe Description ACPI version ? ? Select ? ? Select I	P pointers ed System Tables. Di n has some  Screen tem e Option al Help
				ESC Exit	IIIG EXIL

Feature	Option	Description
Advanced ACPI Configuration	on	
	ACPI v3.0	Set this value to allow or prevent
ACPI Version Features	ACPI v2.0	the system to be complaint with
	ACPI v1.0	the ACPI 2.0 specification.
ACPI APIC Support	Enabled	This option allows you to define
ACFI AFIC Support	Disabled	whether or not to enable ACPI management features.
ACPI SRAT Table	Enabled	Enable or disable the building of
	Disabled	ACPI SRAT Table.
AMI OFMB table	Enabled	Set this value to allow the ACPI BIOS to add a pointer to an OEMB table in the Root System Description Table (RSDT) table.
TAME CEME (ABIO	Disabled	Note: OEMB table is used to pass POST data to the AMI code during ACPI O/S operations.
Headless mode	Enabled	Enable or disable Headless
Headless mode	Disabled	operation mode through ACPI.

## 3.5.7 - Event Logging details Sub-Menu

	BIOS	Setup Uti	ility	
Main Advanced	PCI/PnP	Root	Security	Chinset Exit
Event Logging details				View all unread events on the Event Log.
View Event Log Mark All Events as Read Clear Event Log Event Log Statistics				? ? Select Screen ? ? Select Item +/- Change Option Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit

Feature	Option	Description
Event Logging details		
View Event Log		Views all unread events on the Event Log
Mark All Events as Read	OK Cancel	Marks all unread events as read
Clear Event Log	OK Cancel	Erases all of events.
Event Log Statistics		View details on the count of total unread events. Other stats include size occupied and size free. (in terms of event

## 3.5.8 - Hyper Transport Configuration Sub-Menu

You can use this screen to view the Hyper Transport Configuration Menu. Use the Plus and Minus (+/-) keys to change the value of the selected option. The settings are described on the following pages.

BIOS Main <b>Advanced</b> PCI/PnP	Setup Utility Boot Security	Chipset Exit
Hyper Transport Configuration		The Hyper Transport link will run at this
CPU1: CPU2 HT Link Speed CPU1: CPU2 HT Link Width	[N/A] [N/A]	speed if it is slower than or equal to the system clock and the board is capable.
CPU0: HT2000 HT Link Speed	[Auto]	·
CPU0: HT2000 HT Link Width	[Auto]	? ? Select Screen
HT2000: HT1000 HT Link Speed	[Auto]	? ? Select Item
HT2000: HT1000 HT Link Width	[Auto]	+/- Change Option F1 General Help F10 Save and Exit

Feature	Option	Description			
Hyper Transport Configuration					
CPU1: CPU2 HT Link Speed	200MHz 400MHz 600MHz 800MHz 1GHz	Specifies CPU1 to CPU2 Hyper Transport Link Clock frequency. If CPU2 is absent, the selection item will be hidden.			
CPU1: CPU2 HT Link Width	2 Bit 4 Bit 8 Bit 16 Bit	Specifies CPU1 to CPU2 Hyper Transport Link Data width. If CPU2 is absent, the selection item will be hidden.			
CPU0: HT2000 HT Link Speed HT2000: HT1000 HT Link Speed	Auto 200MHz 400MHz 600MHz 800MHz	The Hyper Transport link will run at this speed if it is slower than or equal to the system clock and the board is capable.			
CPU0: HT2000 HT Link Width HT2000: HT1000 HT Link Width	Auto 2 Bit 4 Bit	The Hyper Transport link will run at this width.			

## 3.5.9 - Hardware Health Configuration Sub-Menu

You can use this screen to view the Hardware Health Configuration Settings. Use the up and down arrow  $(\Upsilon^{\downarrow} \lor)$  keys to select an item. Use the Plus and Minus  $(H^{\downarrow})$  keys to change the value of the selected option. The settings are described on the following pages.

BIOS Setup Utility			
Main Advanced PCI/PnF	Root Security	Chipset Exit	
Hardware Health Configuration		Enables Hardware Health Monitoring	
H/W Health Function FAN Select CPU FAN1, FAN1, 2 Power Control CPU FAN2, FAN3, 4 Power Control FAN Fail LED Indicator	[Enabled] [4Pin FAN] [Disabled] [Disabled] [Disabled]	Device.	
Hardware Health Event Monitoring		? ? Select Screen ? ? Select Item	
▶ Mainboard Voltages Report	•	+/- Change Option Tab Select Field F1 General Help	
CPU1 Temperature	:xx C/ xxx F	F1 General Help F10 Save and Exit	
CPU2 Temperature	:xx C/ xxx F	ESC Exit	
AMB1 Temperature	:xx C/ xxx F :xx C/ xxx F		
AMB2 Temperature	:XX C/ XXX F		
CPU FAN1 Speed	:xxxx RPM		
CPU FAN2 Speed	:xxxx RPM		
FAN1 Speed	:xxxx RPM		
FAN2 Speed	:xxxx RPM		
FAN3 Speed	:xxxx RPM		
FAN4 Speed	:xxxx RPM :xx C/ xxx F		
FAN5 Speed FAN6 Speed	:xx C/ xxx F :xx C/ xxx F		
1 7140 Opecu	0/ 1		

Feature	Option	Description		
Hardware Health Configuration				
H/W Health Function	Enabled	Enables Hardware Health Monitoring Device.		
n/w nealth runction	Disabled			
	4Pin FAN	Selects the FAN type.		
FAN Select	3Pin FAN			

Feature	Option	Description			
Hardware Health Conf	Hardware Health Configuration				
CPU FAN1, FAN1, 2	Enabled	FAN power duty cycle is auto dynamic programmed in selected temperature range. Disabled: Fan Power On.			
Power Control  Disabled		Enabled: Fan Power Duty Cycle= 30%(40°C)- 100%(60°C), see CPU temperature			
CPU FAN2, FAN3, 4	Enabled	FAN power duty cycle is auto dynamic programmed in selected temperature range.  Disabled: Fan Power On.			
Power Control	Disabled	Enabled: Fan Power On:  Enabled: Fan Power Duty Cycle=30%(30°C)-  100%(43°C), see mainboard temp.			
FAN Fail LED Indicator	Enabled Disabled	Enabled: Any FAN speed less than 800 RPM, the FAN Fail LED will be lighted.			

Feature	Option	Description			
Hardware Health Event Mon	Hardware Health Event Monitoring				
Mainboard Voltages Report	read only	Displays Volt age for CPU,			
CPU1 Temperature	read only	Displays CPU Temperature			
CPU2 Temperature		and FAN Speed.			
AMB1 Temperature					
AMB2 Temperature					
CPU FAN1 Speed CPU FAN2 Speed					
FAN1/2/3/4/5/6 Speed					

3.5.9.1 - Mainboard Voltages Report Sub-Menu

BIOS Setup Utility				
Main Advanced  Board Voltages Report	PCI/PnP Boot Security	? ? Select Screen		
CPU1 Vdimm CPU2 Vdimm CPU2 Vdimm CPU3 Vdore CPU2 Voore +V3.3 (SB) +3VDU +V5 (SB) VCC VCC +12V (for cpu1 voore) +12V (for cpu2 voore)	: xxxx V : xxxx V	? ? Select Item +/- Charge Option Tab Select Field FF General Help F10 Save and Ext ESC Exit		

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## 3.5.10 MPS Configuration Sub-Menu

You can use this screen to select MPS revision. Use the up and down arrow  $(\uparrow/\downarrow)$  keys to select an item. The settings are described on the following pages.

Main A	Advanced		Setup Uti Boot	lity Security	Chipset	Exit
MPS Configura		POWFIIF	Boot	Security		S Revision.
MPS Revision		[1.4]	I			et Item nge Option eral Help

Feature	Option	Description
MPS Configuration		
	1.1	l
MPS Revision	1.4	Allows user to select MPS revision.

following pages.

BIOS Setup Utility							
Main Advanced	PCI/PnP	Boot	Security	Chipset	Exit		
PCI Express Configuration	on			Express Li			
Active State Power -Manage	ment	[Di	sabled]	link power	states.		
				? ? Sele	ct Screen		
				? ? Selec	ct Item		
					nge Option eral Help		
				F10 Save	e and Exit		

Feature	Option	Description	
PCI Express Configuration	n		
Active State Power -	Enabled	Enabled/Disabled PCI Express L0s and L1 link power states.	
Management	Disabled		

**3.5.12 AMD PowerNow Configuration Sub-Menu**You can use this screen to enable AMD PowerNOw support. Use the up and down arrow  $( \uparrow \! / \, \downarrow \! )$  keys to select an item. The settings are described on the following pages.

	BIOS Setup Utility							
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit		
AMD Power	Now Configu	ration			Enabled/Disa PowerNow.	abled		
PowerNow		[Disabl	ed]		? ? Select I ? ? Select I +/- Change F1 Genera F10 Save a ESC Exit	tem e Option al Help		

Feature	Option	Description	
AMD PowerNow Configur	ation		
	Enabled		
PowerNow	Disabled	Enabled/Disabled Po werNow	

## 3.5.13 - Remote Access Configuration Sub-Menu

You can use this screen to view the Remote Access Configuration Menu. This feature allows access to the Server remotely via serial port. Use the up and down arrow (\*/-\psi) keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option. The settings are described on the following pages.

BIOS Main <b>Advanced</b> PCI/PnP	Setup Utility Boot Security	Chipset Exit
Configure Remote Access type and	parameters	Select remote access type.
Remote Access [	Disabled]	? ? Select Screen ? ? Select Item +/- Change Field F1 General Help F10 Save and Exit ESC Exit

Feature	Option	Description			
Configure Remote Access	ace type and parameters				
Remote Access	Enabled	Enables remote access to system			
Remote Access	Disabled	through serial port.			

## 3.5.14 - USB Configuration Sub-Menu

You can use this screen to view the USB Configuration Menu. Use the up and down arrow  $(\gamma/\psi)$  keys to select an item. Use the Plus and Minus  $({\it H}')$  keys to change the value of the selected option. The settings are described on the following pages.

	BIOS	Setup Uti	ility	
Main Advanced	PCI/PnP	Root	Security	Chipset Exit
USB Configuration				Enables USB host controllers.
Module Version - X.XX.X-X	(X.X			1
				? ? Select Screen
USB Devices Enabled:				? ? Select Item
None				+/- Change Option F1 General Help
Legacy USB Support	[Enal	oled]		F10 Save and Fxit
BIOS EHCI Hand-Off	[Enat	oled]		ESC Exit

Feature	Option	Description	
USB Configuration			
	Disabled	Enables support for legacy USB.	
Legacy USB Support	Enabled		
B100 E110111 1011	Enabled	This is a work around for OSes without EHCI hand-off support.	
BIOS EHCI Hand-Off	Disabled	The EHCI ownership change	

## 3.5.15 Device & PCI Slots Configuration Sub-Menu

You can use this screen to enable the onboard devices and PCI slots. Use the up and down arrow (  $\uparrow / \downarrow$ ) keys to select an item. The settings are described on the following pages.

Main Advanced		Setup Util Boot	ity Security	Chipset Exit
Onboard Device and PCI	Enabled Disabled			
Onboard VGA Onboard LAN1, LAN2 Devic Onboard LAN1 OP-RC Onboard LAN2 OP-RC Onboard LAN3 Device Onboard LAN3 OP-RC	DM DM	[Enabled] [Enabled] [Disabled [Disabled] [Enabled] [Disabled	  ]  ]	? ? Select Screen ? ? Select Item +/- Change Option F1 General Help F10 Save and Exit ESC Exit

Feature	Option	Description
MPS Configuration		
Onboard VGA	Disabled	Enabled/Disabled VGA controller
Olibbaid VGA	Enabled	Eliabled/bisabled VGA controller
Onboard LAN1, LAN2 Devices	Disabled	Enabled/Di sabled LAN controller
Onboard LAN3 Device	Enabled	Enabled/Di sabled EAN controller
Onboard LAN1 OP-ROM	Disabled	
Onboard LAN2 OP-ROM Onboard LAN2 OP-ROM	Enabled	Executed LAN OPROM or not

## 3.6 -BIOS PCI/PnP Menu

You can use this screen to view PnP (Plug & Play) BIOS Configuration Menu. This menu allows the user to configure how the BIOS assigns resources & resolves conflicts. Use the up and down arrow  $(\uparrow \land \psi)$  keys to select an item. Use the Plus and Minus  $(+\cdot)$  keys to change the value of the selected option. The settings are described on the following pages.

BIOS S Main Advanced <b>PCI/PnP</b>	Setup Utility Boot Security	/ Chipset Exit
Advanced PCI/PnP Settings	Clear NVRAM during System Boot.	
WARING: Setting wrong values in below cause system to malfunction.  Clear NVRAM Plug & Play O/S PCI Latency Timer PCI Bus Scan Order Allocate IRG to PCI VGA	? ? Select Screen ?? Select Item +/- Change Option F1 General Help F10 Save and Exit ESC Exit	
Palette Snooping PCI IDE BusMaster	[Yes] [Disabled] [Disabled]	

Feature	Ontion	Description
Advanced PCI/PnP Settings		
Clear NVRAM	No Yes	Clears NVRAM during system Boot.
Plug & Play OS	Yes	No: lets the BIOS configure all the devices in the system. Yes: lets the operating system
Flug & Flay OS	No	configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.
	32	This setting controls how many
	64	PCI clocks each PCI device can hold the bus before another PCI
PCI Latency Timer	96	device takes over. When set to
	128	higher values, every PCI device
	160	can conduct transactions for a longer time and thus improve the
	192	effective PCI bandwidth.
	224	Values in units of PCI clocks for
	248	PCI device latency timer register.
PCI Bus Scen Order	Ascent	Ascent: Scan PCI bus from bus 0 to maximum.
POI Bus Scell Older	Descent	Descent: Scan PCI bus from
Allerent IDO to DOLVOA	Yes	Yes: assigns IRQ to PCI VGA card
Allocate IRQ to PCI VGA	No	if card requests IRQ.
Palette Snooping	Disabled	This is the default setting and should not be changed unless the VGA card manufacturer requires Palette Snooping to be Enabled.
Palette Shooping	Enabled	Enabled: informs the PCI devices that an ISA graphics device is installed in the system so the card will function correctly.
PCI IDE BusMast er	Disabled Enabled Reserved	Enabled: BIOS uses PCI bus mastering for reading / writing to IDE drives.

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## 3.7 - BIOS Boot Menu

You can display Boot Setup option by highlighting it using the Arrow ( $\uparrow \land \lor \downarrow$ ) keys and pressing Enter. The settings are described on the following pages.

BIOS Setup Utility Main Advanced PCI/PnP <b>Boot</b> Security	Chipset Exit
Boot Settings	Configures settings during System Boot.
Boot Settings Configuration     Boot Device Priority     Removable Drives     CD/DVD Drives	? ? Select Screen ? ? Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit

## 3.7.1 - Boot Settings Configuration Sub-Menu

Use this screen to select options for the Boot Settings Configuration. Use the up and down arrow  $(\uparrow 1/4)$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

Main Advanced	BIOS Setup PCI/PnP Bo		Security	Chipset	Exit
Boot Settings Configuration		Allows BIOS to skip			
Quick Boot Quiet Boot Add On ROM Display Mode Boot up Num-Lock PS/2 Mouse Support Wait for F-1 if Error Hit 'DEL' Message Display Interrupt 19 Capture	[Disabl [Disabl [Force [On] [Auto] [Enabl [Enabl [Disabl	ed] BIOS] ed] d]		booting. This decrease the needed to be system.  ? ? Select ?? Select +/- Chang F1 General decrease the control of the control	s will e time oot the Screen

Feature	Option	Description
<b>Boot Settings Configuration</b>	n	
Quick Boot	Enabled	This option allows user bypass BIOS
quion boot	Disabled	self test during POST.
Quiet Boot	Disabled	Disabled: displays normal POST messages.
Quiet Door	Enabled	Enabled: displays OEM log instead of POST messages
Add On ROM Display	Force BIOS	Allows user to force BIOS/Option ROM
Mode	Keep Current	of add-on cards to be displayed during quiet boot.
Boot up Num-Lock	On Off	Selects Power-on state for Numlock.
	Enabled	
PS/2 Mouse Support	Disabled	Selects support for PS/2 Mouse.
	Auto	
Wait for 'F 1' If Error	Enabled	Waits for F1 key to be present if error
Walt for 1 1 ii Eiror	Disabled	occurs.
Hit 'DEL' Message Display	Enabled	Displays "Press DEL to run Setup" in
Till DEE Wessage Display	Disabled	POST.
Interrupt 19 Capture	Disabled	Enabled: allows option ROMs to trap
interrupt 15 Capture	Enabled	interrupt 19.

## 3.7.2 - Boot Device PrioritySub-Menu

Use this screen to select options for the Boot Device Priority. Use the up and down arrow  $(\uparrow \land \downarrow)$  keys to select an item. Use the Plus and Minus  $(+ \land -)$  ke ys to change the value of the selected option.

Main Advanced	BIOS Setup Utility PCI/PnP Boot Security	Chipset Exit
Boot Device Priority		Specifies the boot sequence from the
1st Boot Device 2nd Boot Device	[XX,XXX-XXXXXXXX]  [XX,XXX-XXXXXXXX]  A device enclic parenthesis he been disabled corresponding menu.	
		? ? Select Screen ? ? Select Item +/- Change Option F1 General Help F10 Save and Exit ESC Exit

Feature	Option	Description
<b>Boot Device Priority</b>		
1st Boot Device	xx,xxx-xxxxx:xxx	Settings for boot priority.
2nd Boot Device	xx,xxx-xxxxx:xxx Disabled	These can be customized depending on your

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## 3.7.3 - Removable Drives Sub-Menu

Use this screen to select options for the Removable Drives. Use the up and down arrow (h/4) keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

			Setup Util			
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
Removable	Drives				Specifies the	
1st Drive		[xxxxxx	XXXXXXXXX	xxx]	sequence f available d	
					? ? Selec	ot Caroon
					? ? Selec	
						ge Option eral Help
					ESC Exit	anu EXII

Feature	Option	Description
Removable Drives		
	xx,xxx-xxxxx:xxx	Specifies the boot sequence for removable drive booting.
1st Drive	Disabled	This option will show all removable devices.

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## 3.7.4 - Removable Drives Sub-Menu

Use this screen to select options for the CD/DVD Drives. Use the up and down arrow (h/4) keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

			Setup Util			
Main	Advanced	PCI/PnP	Boot	Security	Chipset	Exit
CD/DVD Driv	es				Specifies the	
1st Drive		[xxxxxx	OXXXXXXXX	xxx]	sequence f available d	
						t Item ge Option eral Help

Feature	Option	Description
CD/DVD Drives		
	xx,xxx-xxxxx:xxx	Specifies the boot sequence for removable drive booting.
1st Drive	Disabled	This option will show all CD/DVD devices.

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## 3.8 - BIOS Security Menu

The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is entered, using either the Supervisor password or User password. The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must clear CMOS and reconfigure.

BIOS Setup Utility Main Advanced PCI/PnP Boot <b>Security</b>	Chipset Exit
Security Setting s	Install or change the password.
Supervisor Password : Not Installed User Password : Not Installed	? ? Select Screen
Change Supervisor Password	+/- Change Option
Change User Password  Boot Sector Virus Protection [Disabled]	F1 General Help F10 Save and Exit ESC Exit

Feature	Option	Description	
Security Setting s			
Supervisor Password:	Not Installed Installed	If the password has been set, Installed displays. If no password is set. Not Installed displays.	
User Password:	Not Installed Installed	If the password has been set, Installed displays. If no password is set. Not Installed displays	
Change Supervisor		Selects this option to change or install Supervisor Password	
Change User Password		Selects this option to change or install User Password	
Boot Sector Virus Protection	Disabled	When it is set to [Enabled], BIOS will issue a virus warning message and beep if a write to the boot sector or the partition while of the HIDS is externated.	
	Enabled		

## 3.9 - BIOS Chipset Menu

This menu allows the user to customize functions of the AMD Chipsets. North Bridge configuration contains options for Memory & CPU settings. South Bridge configuration contains options for SM Bus & USB. Additional configuration for the AMD8131 PCI-X Tunnel is available in the PCI-X Configuration Menu. Select a menu by highlighting it using the Arrow (  $\uparrow\!\!\!/\, \downarrow\!\!\!/ \rangle$  keys and pressing Enter. The settings are described on the following pages.

BIOS Setup Utility					
Main	Advanced	PCI/PnP	Root	Security	Chinset Frit
▶ HT2000 S	ige Configurat System I/O Co South Bridge C	nfiguration		,	Options for NB.  ? ? Select Screen ? ? Select Item +/- Change Option Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit

# 3.9.1 - North Bridge Chipset Configuration Sub-Menu

This menu gives options for customizing memory & Hypertransport setting s. Select a menu by highlighting it using the Arrow  $(\uparrow \!\! / \!\! \downarrow)$  keys and pressing Enter. The settings are described on the following pages.

Main Advanced	BIOS Setup Utility PCI/PnP Boot Security	Chipset Exit
NorthBridge Chipset Cor	? ? Select Screen ? ? Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit	
➤ Memory Configuration ➤ ECC Configuration ➤ IOMMU Option Configuration		
, .	:XXX MHz	ESC Exit
CAS latency (Tcl) RAS/CAS Delay (Trcd)		
Min Active RAS (Tras)		
Row Precharge Time (Trp)		
RAS/RAS Delay (Trrd)		
Row Cycle (Trc) Row Refresh Cycle (Trfc)		
Read Write Delay (Trwt)		
Read Preamble		
Asynchronous Latency	:X ns	

Feature	Option	Description				
NorthBridgeChipset Configuration						
Memory CLK	Read only	It shows the clock frequency of the installed SDRAM.				
CAS Latency (Tcl)	Read only	This controls the timing delay (in clock cycles) before SDRAM starts a read command after receiving it.				
RAS/CAS Delay (Trcd)	Read only	When DRAM is refreshed, both rows and columns are addressed separately. This setup item allows you to determine the timing of the transition from RAS (row address strobe) to CAS (column address strobe). The less the clock cycles, the faster the DRAM				

Feature	Ontion	Description
NorthBridgeChipset C		Tiescriminin
Min Active RAS (Tras)	Read only	This setting allows you to select the number of clock cycles allotted for the RAS pulse width, according to DRAM specifications. The less the clock cycles, the faster the DRAM performance.
Row Precharge Time (Trp)	Read only	This item controls the number of cycles for Row Address Strobe (RAS) to be allowed to precharge. If insufficient time is allowed for the RAS to accumulate its chage before DRAM refresh, refresh may be incomplete and DRAM may fail to retain data. This item applies only when synchronous DRAM is a statled in the system.
RAS/RAS Delay (Trrd)	Read only	Auto uses hardware compens ation values. Other values add to or subtract from hardware generated value. Recommended setting is Auto.
Row Cycle (Trc)	Read only	Bits 7-4. RAS#-active to RAS#-active
Row Refresh Cycle	Read only	Bits 11-8. Auto-refresh-active to
Read Write Delay (Trwt)	Read only	Bits 6-4. Specifies the read-to-write delay. This is not a DRAM-specified timing parameter, but must be considered due to routing latencies on the clock forwarded bus. It is counted from the first address bus slot that was not associated with part of the read burst.
Read Preamble	Read only	Bits 11-8. The time prior to the max- read DOS-rectum when the DOS receiver should be turned on. This is specified in units of 0.5ns. The controller needs to know when to enable its DOS receiver in anticipation of the DRAM DOS driver turning on for a read. The controller will disable its DOS receiver until the read preamble time and then enable its DOS receiver while the DRAM asserts DOS
Asynchronous Latency	Read only	Bits 3-0. This filed should be loaded with a 4-bit value equal to the maximum asynchronous latency in the

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# 3.9.1.1 - Memory Configuration Sub - Menu

	S Setup Utility	
Main Advanced PCI/PnP  Memory Configuration	Root Security	MEMCLK can be set by the code using
Memclock Mode MCT Timing Mode User Config Mode Burst Length HardWare Memory Hole	[Auto] [Auto] [Auto] [4 Beats] [Enabled]	AUTO, or if you use LIMIT, you can set one of the standard values.  ? ? Select Screen ? ? Select Item
CPU1 Mem DQ Driver Strength CPU2 Mem DQ Driver Strength	[No Reduction] [No Reduction]	+/- Change Option F1 General Help F10 Save and Exit ESC Exit

Feature	Option	Description
Memory Configuration		
Memclock Mode	Limit	MEMCLK can be set by the code using AUTO, or if you use LIMIT,
Welliclock Wode	Auto	you can set one of the standard
MCT Timing Mode	Manual Auto	Allows user to configure the MCT Timing Mode manually.
User Config Mode	Manual Auto	Allows user to set the User Config Mode manually.
	8 Beats	Burst length can be set to 8 or 4
Burst Length	4 Beats	beats. 64 bit DQ must use 4 beats.
	2 Beats	
HardWare Memory Hole	Disabled	Allows user to enable hardware
	Enabled	memory remapping around memory hole.
CPU1 Mem DQ Driver	No Reduction	This field controls the drive strength
Strength	-15%	reduction of the Memory DQ pins.
CPU2 Mem DQ Driver Strength	-30%	
Strength	E00/	

**3.9.1.2 –ECC Configuration Sub-Menu**This menu allows the user to configure ECC setup for system & DRAM. Use the up and down arrow ( ↑/ ↓) keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

BIOS Main Advanced PCI/PnP	S Setup Utility Boot Security	Chipset Frit
ECC Configuration	,	DRAM ECC allows hardware to report and
DRAM ECC Enable MCA DRAM ECC Logging ECC Chip Kill DRAM SCRUB REDIRECT DRAM BG Scrub L2 Cache BG Scrub Data Cache BG Scrub	[Enabled] [Disabled] [Enabled] [Disabled] [Disabled] [Disabled] [Disabled]	correct memory errors automatically maintaining system integrity.  ? ? Select Screen ? ? Select ttem +/- Change Option F1 General Help F10 Save and Exit ESC Evit

Feature	Ontion	Description
ECC Configuration		
DRAM ECC Enable	Enabled	DRAM ECC allows hardware to report and correct memory errors
	Disabled	automatically maintaining system integrity.
MCA DRAM ECC	Disabled	Enables MCA DRAM ECC Logging
Logging	Enabled	Reporting.
ECC Chip Kill	Disabled Enabled	ECC Chip Kill
DRAM SCRUB	Disabled	DRAM SCRUB REDIRECT allows the system to correct DRAM ECC
REDIRECT	Enabled	errors immediately when they occur, even if background scrubbing is on.
	Disabled	DRAM scrubbing corrects memory
	40ns	errors so later reads are correct.
	80ns	Doing this while memory is not being
	160ns	used improves performance.
	320ns	Note: When AMD's node interleave
	640ns	feature is enabled, BIOS will force DRAM scrub off.
	1.28us	DRAW SCIUD OII.
DRAM BG Scrub	2.56us	
DRAM BG Scrub	5.12us	
	10.2us	
	20.5us	
	41.0us	
	81.9us	
	163.8us	
	327.7us	
	655.4us	
	Disabled	Allows the L2 Data Cache RAM to
	40ns	be corrected while idle.
	80ns	
	160ns	1
	320ns	1
	640ns	1
	1.28us	
1	2.56us	1
L2 Cache BG Scrub	5.12us	1
	10.2us	1
	20.5us	1
	41.0us	1
	81.9us	1
	163.8us	
	327.7us	1
I	655 Aug	1

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Feature	Ontion	Description
ECC Configuration		
Data Cache BG Scrub	Disabled 40ns 80ns 160ns 320ns 640ns 1.28us 2.56us 1.12us 10.2us 20.5us 41.0us 81.9us 163.8us 327.7us	Allows the L1 Data Cache RAM to be corrected while idle.
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# 3.9.1.3 - IOMMU Configuration Sub - Menu

	BIOS Setup Utility					
Main	Advanced	PCI/PnP	Root	Security	Chipset	Exit
IOMMU Mode	9		[Disable	id]	Set GART's systems with or disable a Some OSes valid GART operation, I present, sel appropriate ensure prop operation.	hout AGP, Itogether. s require for proper If AGP is ect option to
					? ? Select +/- Chang F1 Gener	t Screen Item ge Option ral Help and Exit

Feature	Option	Description
IOMMU Configuration		
	AGP Present Disabled 32 MB	Set GART size in systems without AGP, or disable altogether. Some OSes require valid GART for proper
IOMMU Mode	64 MB 128 MB	operation, If AGP is present, select appropriate option to ensure proper
	512 MB	AGP operation.

# 3.9.2 - HT2000 System I/O Configuration Sub-Menu

This menu allows the user to configure HT2000 System I/O Submenu . Use the up and down arrow (  $\uparrow / \downarrow \rangle$  keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

Main Advanced	BIOS PCI/PnP	Setup U		Chinset Fxit
HT2000 Chipset Configur	ation			Enable/Disable EXB1
Split PCI -E Master 1 to 2 (x Split PCI -E Master 3 to 2 (x			Disabled] Disabled]	Split ? ? Select Screen ? ? Select Item +/- Change Option F1 General Help F10 Save and Exit ESC Exit

Feature	Option	Description
Chipset Configuration		
Split PCI -E Master 1 to 2	Enabled	
(x4)	Disabled	Enabled/Disable EXB1 Split
Split PCI -E Master 3 to 2	Enabled	5 5V22.0 !!
(x4)	Disabled	Enabled/Disable EXB3 Split

## 3.9.3 - HT1000 SouthBridge Chipset Configuration Sub - Menu

This menu allows the user to enable SM Bus 2.0 controller. Use the up and down arrow ( $\uparrow \land \downarrow$ ) keys to select an item. Use the Plus and Minus (+/-) keys to change the value of the selected option.

BIOS Setup Utility					
Main	Advanced	PCI/PnP	Root	Security	Chinset Frit
Power Control After Power Fail		[Disabled] [Enabled] ? ? Select Scr	Enabled Former State ? ? Select Screen		
	ner je Chipset Co	onfiguration		Disabledj	? ? Select Item +/- Change Option F1 General Help
Hide XIOAPI Power Butto	IC PCI Function	ons		Enabled] Enabled]	F10 Save and Exit ESC Exit

Feature Chinest Configuration	Option	Description
Power Control After Power Fail	Former State  Disabled	
Resume on RTC Alarm	Enabled Disabled	
Resume on PME#	Enabled Disabled	
Watchdog Timer	Enabled Disabled	Once timer is activated, it can only be disabled by system shutdown.  The timer starts down-count at the system power on

Feature	Option	Description			
South ridge Chinest Configuration					
Hide XIOAPIC PCI	Enabled	Hide XIOAPIC PCI functions.			
Functions	Disabled	Hide XIOAPIC PCI functions.			
Power Button Install Off	Enabled	Disable or enable power button instant off.			

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## 3.10 - BIOS Exit Menu

BIOS Setup Utility Main Advanced PCI/PnP Boot Sec	urity Chipset Exit
Exit Options	Exit system setup after saving the changes.
Save Changes and Exit Discard Changes and Exit Discard Charges Load Optimal Defaults Load Failsafe Defaults	F10 key can be used for this operation.  ? ? Select Screen ? ? Select Item Enter Go to Sub Screen F1 General Help
	F10 Save and Exit ESC Exit

# Save Changes and Exit

Use this option to exit setup utility and re-boot.
All new selections you have made are stored into CMOS.
System will use the new settings to boot up.

## **Discard Changes and Exit**

Use this option to exit setup utility and re-boot.

All new selections you have made are not stored into CMOS. System will use the old settings to boot up.

# Discard Changes

Use this option to restore all new setup values that you have made but not saved into CMOS.

## **Load Optimal Defaults**

Use this option to load default performance setup values.

Use this option when system CMOS values have been corrupted or modified incorrectly.

## Load Failsafe Defaults

Use this option to load all default failsafe setup values.

Use this option when troubleshooting.

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# **Chapter 4: Diagnostics**

Note: if you experience problems with setting up your system, always check the following things in the following order:

## Memory, Video, CPU

By checking these items, you will most likely find out what the problem might have been when setting up your system. For more information on troubleshooting, check the TYAN website at: <a href="http://www.tvan.com">http://www.tvan.com</a>.

## 4.1 Beep Codes

Fatal errors, which halt the boot process, are communicated through two kinds of audible beeps.

 A single long beep followed by two short beeps: It indicates that a video error has occurred and the BIOS can't initialize the video screen to display and additional info.

•A single long beep repeatedly: This indicates that a DRAM error has occurred.

The most common type of error is a memory error.

Before contacting your vendor or TYAN Technical Support, be sure that you note as much as you can about the beep code length and order that you experience. Also, be ready with information regarding add -in cards, drives and O'S to speed the support process and come to a quicker solution.

## 4.2 Flash Utility

Every BIOS file is unique for the motherboard it was designed for. For Flash Utilities, BIOS downloads, and information on how to properly use the Flash Utility with your motherboard, please check the TYAN web site: http://www.tyan.com/

Note: Please be aware that by flashing your BIOS, you agree that in the event of a BIOS flash failure, you must contact your dealer for a replacement BIOS. There are no exceptions. TYAN does not have a policy for replacing BIOS chips directly with end users. In no event will TYAN be held responsible for damages done by the end user.

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# 4.3 AMIBIOS Post Code

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize
	BIOS, POST, Runtime data area. Also initialize BIOS modules on
	POST entry and GPNV area. Initialized CMOS as mentioned in the
	Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and
	CMOS checksum is OK. Verify CMOS checksum manually by
	reading storage area. If the CMOS checksum is bad, update CMOS
	with power-on default values and clear passwords. Initialize status
	register A.
	Initializes data variables that are based on CMOS setup questions.
	Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and
	interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install
	the POSTINT1Ch handler. Enable IRQ -0 in PIC for system timer
	interrupt.
	Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
08	Initializes the CPU. The BAT test is being done on KBC. Program
	the keyboard controller command byte is being done after Auto
	detection of KB/MS using AMI KB-5.
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
OC	
	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the
	Testing and initialization of different Input Devices. Also, update the Kernel Variables.
	Testing and initialization of different Input Devices. Also, update the Kernel Variables.  Traps the INT 09h vector, so that the POST INT09h handler gets
	Testing and initialization of different Input Devices. Also, update the Kernel Variables.  Traps the INT 09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT 09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables.  Traps the INT 09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and silent logo modules.  Early POST initialization of chipset registers.
0E 13 24	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT 08h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules. Early POST initialization of chipset registers.  Locompress and initialize any platform specific BIOS modules.
0E 13 24 30	Testing and initialization of different Input Devices. Also, update the Kernel Variables.  Traps the INT 09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.  Early POST initialization of chisest registers.  Uncompress and initialize any platform specific BIOS modules.  Initialize System Management Interrupt.
0E 13 24	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT 09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and silent logo modules.  Early POST initialization of chipset registers. Uncompress and initialize any platform specific BIOS modules. Initialize System Management Interrupt. Initialize different devices through DIM.
0E 13 24 30 2A	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT 09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.  Early POST initialization of chipset registers.  Uncompress and initialize any lettform specific BIOS modules.  Initialize System Management Interrupt.  Initializes different devices through DIM.  See DIM Code Checkpoints section of document for more information.
0E 13 24 30	Testing and initialization of different Input Devices. Also, update the Kernel Variables.  Traps the INT '09 hector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.  Farly POST initialization of chioset registers.  Uncompress and initialize any platform specific BIOS modules.  Initialize System Management Interrupt.  Initializes different devices through DIM.  See DIM Code Checkpoints section of document for more information.  Initializes different devices. Detects and initializes the video adapter
0E 13 24 30 2A 2C	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT 09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.  Early POST initialization of chinset renisters.  Honcompress and initialize any platform specific BIOS modules. Initialize System Management Interrupt.  Initializes different devices through DIM.  See DIM Code Checkpoints section of document for more information. Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
13 24 30 2A 2C 2F	Testing and initialization of different Input Devices. Also, update the Kernel Variables.  Traps the INT '09N vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.  Early POST initialization of chinset registers.  Uncompress and initialize any platform specific BIOS modules.  Initialize System Management Interrupt.  Initializes different devices through DIM.  See DIM Code Checkpoints section of document for more information.  Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
0E 13 24 30 2A 2C	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT 09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.  Early POST initialization of chipset registers.  Lincompress and initialize any platform specific BIOS modules.  Initialize System Management Interrupt.  Initializes different devices through DIM.  See DIM Code Checkpoints section of document for more information.  Initializes different devices. Detects and initializes the video adapter installed in the sy stem that have optional ROMs.  Initializes all the nutbrut devices.  Allocate memory for ADM module and uncompress it. Give control to
13 24 30 2A 2C 2F	Testing and initialization of different Input Devices. Also, update the Kemel Variables. Traps the INT 09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.  Early POST initialization of chioset registers.  Uncompress and initialize any platform specific BIOS modules.  Initialize System Management Interrupt.  Initializes different devices through DIM.  See DIM Code Checkpoints section of document for more information.  Initializes different devices. Detects and initializes the video adapter installed in the sy stem that have optional ROMs.  Initializes all the nutruit devices.  Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for
13 24 30 2A 2C 2F	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT 09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.  Early POST initialization of chipset registers.  Lincompress and initialize any platform specific BIOS modules.  Initialize System Management Interrupt.  Initializes different devices through DIM.  See DIM Code Checkpoints section of document for more information.  Initializes different devices. Detects and initializes the video adapter installed in the sy stem that have optional ROMs.  Initializes all the nutbrut devices.  Allocate memory for ADM module and uncompress it. Give control to

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Checkpoint	Description
37	Displaying sign-on message, CPU information, setup key message,
0.	and any OEM specific information.
38	Initializes different devices through DIM. See DIM Code Checkpoints
	section of document for more information.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or
	ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor
	in CPU, etc.) successfully installed in the system and update the
	BDA, EBDAetc.
50	Programming the memory hole or any kind of implementat ion that
	needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test.
60	Allocates memory for Extended BIOS Data Area from base memory.  Initializes NUM-LOCK status and programs the KBD typematic rate.
	Initializes NOM-LOCK status and programs the KBD typematic rate.  Initialize Int -13 and prepare for IPL detection.
75 78	Initialize Int - 13 and prepare for IPL detection.  Initializes IPL devices controlled by BIOS and option ROMs.
78 7A	Initializes IPL devices controlled by BIOS and obtion ROMs.  Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.
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85	Log errors encountered during POST.  Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested.
87 8C	Late POST initialization of chipset registers.
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules.
742	Fill the free area in F000h segment with 0FFh. Initializes the
	Microsoft IRQ Routing Table. Prepares the runtime language module.
	Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the
	CPU's before boot, which includes the programming of the MTRR's.
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the
	ADM module.
AB	Prepare BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Passes control to OS Loader (typically INT19h).

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# **Appendix I: SMDC Information**

#### Overview

Tyan Server Management Daughter Card (SMDC) is a powerful yet cost-efficient solution for high-end server management hardware packages. Tyan's goal is to provide remote system monitoring and control even when the operating system is absence or simply fails. This empowers Tyan's server board with advanced industrial-standard features.

Tyan SMDC is a snap-in card that provides essential server management solution. It enables any IT Manager by providing multi-interfaces to access the hardware remotely and perform monitor, control and diagnose activities effectively.

Tyan SMDC is not a peripheral card. Unlike regular peripheral card such as AGP card, Network card or SCSI card, SMDC does not require any hardware specific driver. As long as a standby power comes into the system, SMDC will begin looking after the system.

Tyan SMDC provides diversified methods to communicate with the hardware. IT manager has the flexibility to choose among Keyboard Controller Style (KCS), Block Transfer (BT) style, Intelligent Chassis Management Bus (ICMB), Intelligent Platform Management Bus (IPMB), Emergency Management Port (EMP) and standard IPMI - Over-LAN communication as defined in latest IPMI 1.5 specification.

Tyan SMDC is compatible with all IPMI -compliance software as well as Tyan System Operator $^{TM}$  (TSO) software package.

By adding SMDC, Tyan's server board becomes a highly manageable and IPMI compatible system with all the advanced features suggesting in IPMI Spec.

More detailed information on Tyan's SMDC card can be found on our website: http://www.tyan.com.

## Features of Tyan Server Management



Monitor various system components remotely -such as fans, processor temperature, and more



Remote power on and power off



Console redirect -the ability to view system remotely



Alert and error actions -such as audible beep, e-mail, power down and reboot



SMDC runs on stand-by power -the SMDC will continue to function, even if the system is not powered on

## How SMDC and TSO Work

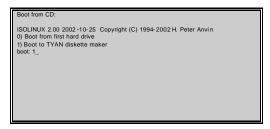
The brief descriptions below will help explain how these items function.

<b>∅</b> →	Agent – a system with SMDC installed The SMDC is installed in the Agent system that uses a compatible/supported Tyan motherboard.
	Manager – manages the Agent The Manger is set up to manage the Agent that has the SMDC. The Manager and Agent should be located in the same place.
	Console – communicates with Manager The Console is used to monitor and control the Agent through the Manager.

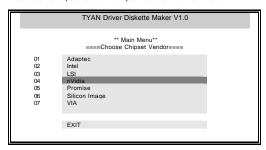
# Appendix II: How to Make a Driver Diskette

Follow the steps below to make a driver diskette from the TYAN driver CD provided.

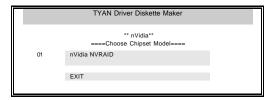
 Start the system and insert the TYAN CD into the CD-ROM drive to boot from CD. You will see the following menu. Then press [1] and [Enter] to boot the system to TYAN diskette maker. (If you would like to boot from hard disk, press 0 and Enter or just wait for 10 seconds to boot automatically from hard disk.).



2. Choose the chipset vender which you need from the main menu.



3. The following picture pops up after selecting the chipset model.



4. After selecting the chipset model, select the OS to start the diskette making.

	TYAN Driver Diskette Maker
	====nVidia NVRAID SATA and RAID Driver====
Diskette =01=	Microsoft Windows 2000 32-bit
Diskette =02=	Microsoft Windows XP 32-bit
Diskette =03=	Microsoft Windows XP 64bit
Diskette =04=	Microsoft Windows 2003 64-bit
	Back

5. Follow the instruction on menu to insert a diskette and press [ENTER].

\Please insert a formatted diskette into A:/ and press [ENTER] Writing image to drive A: Track: 36 Hoad: 8 Sector: 1	

6. Using "ESC" key to quit the TYAN diskette maker. The system will automatically restart.

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# Glossary

ACPI (Advanced Configuration and Power Interface): a power management specification that allows the operating system to control the amount of power distributed to the computer's devices. Devices not in use can be turned off, reducing unnecessary power expenditure.

AGP (Accelerated Graphics Port): a PCI-based interface which was designed specifically for demands of 3D graphics applications. The 32-bit AGP channel directly links the graphics controller to the main memory. While the channel runs only at 66 MHz, it supports data transmission during both the rising and falling ends of the clock cycle, yielding an effective speed of 133 MHz.

ATAPI (AT Attachment Packet Interface): also known as IDE or ATA; a drive implementation that includes the disk controller on the device itself. It allows CD-ROMs and tape drives to be configured as master or slave devices, just like HDDs.

ATX: the form factor designed to replace the AT form factor. It improves on the AT design by rotating the board 90 degrees, so that the IDE connectors are closer to the drive bays, and the CPU is closer to the power supply and cooling fan. The keyboard, mouse, USB, serial, and parallel ports are built in.

Bandwidth: refers to carrying capacity. The greater the bandwidth, the more data the bus, phone line, or other electrical path can carry. Greater bandwidth results in greater speed.

BBS (BIOS Boot Specification): a feature within the BIOS that creates, prioritizes, and maintains a list of all Initial Program Load (IPL) devices, and then stores that list in NYRAM. IPL devices have the ability to load and execute an OS, as well as provide the ability to return to the BIOS if the OS load process fails. At that point, the next IPL device is called upon to attempt loading of the

BIOS (Basic Input/Output System): the program that resides in the ROM chip, which provides the basic instructions for controlling your computer's hardware. Both the operating system and application software use BIOS routines to ensure compatibility.

Buffer: a portion of RAM which is used to temporarily store data; usually from an application though it is also used when printing and in most keyboard drivers. The CPU can manipulate data in a buffer before copying it to a disk drive. While this improves system performance (reading to or writing from a disk drive a single time is much faster than doing so repeatedly) there is the possibility of

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losing your data should the system crash. Information in a buffer is temporarily stored, not permanently saved.

Bus: a data pathway. The term is used especially to refer to the connection between the processor and system memory, and between the processor and PCI or ISA local buses.

**Bus mastering:** allows peripheral devices and IDEs to access the system memory without going through the CPU (similar to DMA channels).

Cache: a temporary storage area for data that will be needed often by an application. Using a cache lowers data access times since the information is stored in SRAM instead of slower DRAM. Note that the cache is also much smaller than your regular memory: a typical cache size is 512KB, while you may have as much as 4GB of regular memory.

Closed and open jumpers: jumpers and jumper pins are active when they are "on" or "closed", and inactive when they are "off" or "open".

**CMOS (Complementary Metal -Oxide Semiconductors):** chips that hold the basic startup information for the BIOS.

**COM port:** another name for the serial port, which is called as such because it transmits the eight bits of a byte of data along one wire, and receives data on another single wire (that is, the data is transmitted in serial form, one bit after another). Parallel ports transmit the bits of a byte on eight different wires at the same time (that is, in parallel form, eight bits at the same time).

DDR (Double Data Rate): a technology designed to double the clock speed of the memory. It activates output on both the rising and falling edge of the system clock rather than on just the rising edge, potentially doubli

**DIMM (Dual In-line Memory Module):** faster and more capacious form of RAM than SIMMs, and do not need to be installed in pairs.

**DIMM bank:** sometimes called DIMM socket because the physical slot and the logical unit are the same. That is, one DIMM module fits into one DIMM socket, which is capable of acting as a memory bank.

DMA (Direct Memory Access): channels that are similar to IRQs. DMA channels allow hardware devices (like soundcards or keyboards) to access the main memory without involving the CPU. This frees up CPU resources for other tasks. As with IRQs, it is vital that you do not double up devices on a single line. Plug-n-Play devices will take care of this for you.

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DRAM (Dynamic RAM): widely available, very affordable form of RAM which looses data if it is not recharged regularly (every few milliseconds). This refresh requirement makes DRAM three to ten times slower than non-recharged RAM such as SRAM.

ECC (Error Correction Code or Error Checking and Correcting): allows data to be checked for errors during run-time. Errors can subsequently be corrected at the same time that they're found.

EEPROM (Electrically Erasable Programmable ROM): also called Flash BIOS, it is a ROM chip which can, unlike normal ROM, be updated. This allows you to keep up with changes in the BIOS programs without having to buy a new chip. TYAN's BIOS updates can be found at http://www.tyan.com

ESCD (Extended System Configuration Data): a format for storing information about Plug-n-Play devices in the system BIOS. This information helps properly configure the system each time it boots.

Firmware: low-level software that controls the system hardware.

Form factor: an industry term for the size, shape, power supply type, and external connector type of the Personal Computer Board (PCB) or motherboard. The standard form factors are the AT and ATX.

Global timer: onboard hardware timer, such as the Real-Time Clock (RTC).

HDD: stands for Hard Disk Drive, a type of fixed drive.

H-SYNC: controls the horizontal synchronization/properties of the monitor.

HyperTransport<sup>™</sup>: a high speed, low latency, scalable point-to-point link for interconnecting ICs on boards. It can be significantly faster than a PCI bus for an equivalent number of pins. It provides the bandwidth and fl exibility critical for today's networking and computing platforms while retaining the fundamental programming model of PCI.

IC (Integrated Circuit): the formal name for the computer chip.

IDE (Integrated Device/Drive Electronics): a simple, self-contained HDD interface. It can handle drives up to 8.4 GB in size. Almost all IDEs sold now are in fact Enhanced IDEs (EIDEs), with maximum capacity determined by the hardware controller.

IDE INT (IDE Interrupt): a hardware interrupt signal that goes to the IDE.

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**I/O (Input/Output):** the connection between your computer and another piece of hardware (mouse, keyboard, etc.)

IRQ (Interrupt Request): an electronic request that runs from a hardware device to the CPU. The interrupt controller assigns priorities to incoming requests and delivers them to the CPU. It is important that there is only one device hooked up to each IRQ line; doubling up devices on IRQ lines can lock up your system. Plug-n-Play operating systems can take care of these details for you

Latency. the amount of time that one part of a system spends waiting for another part to catch up. This occurs most commonly when the system sends data out to a peripheral device and has to wait for the peripheral to spread (peripherals tend to be slower than on board system components).

**NVRAM:** ROM and EEPROM are both examples of Non-Volatile RAM, memory that holds its data without power. DRAM, in contrast, is volatile.

Parallel port: transmits the bits of a byte on eight different wires at the same time.

PCI (Peripheral Component Interconnect): a 32 or 64-bit local bus (data pathway) which is faster than the ISA bus. Local buses are those which operate within a single system (as opposed to a network bus, which connects multiple systems)

PCI PIO (PCI Programmable Input/Output) modes: the data transfer modes used by IDE drives. These modes use the CPU for data transfer (in contrast, DMA channels do not). PCI refers to the type of bus used by these modes to communicate with the CPU.

PCI-to-PCI bridge: allows you to connect multiple PCI devices onto one PCI slot

Pipeline burst SRAM: a fast secondary cache. It is used as a secondary cache because SRAM is slower than SDRAM, but usually larger. Data is cached first to the faster primary cache, and then, when the p rimary cache is full, to the slower secondary cache.

PnP (Plug-n-Play): a design standard that has become ascendant in the industry. Plug-n-Play devices require little set-up to use. Devices and operating systems that are not Plug-n-Play require you to reconfigure your system each time you add or change any part of your hardware.

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PXE (Preboot Execution Environment): one of four components that together make up the Wired for Management 2.0 baseline specification. PXE was designed to define a standard set of preboot protocol services within a client with the goal of allowing networked-based booting to boot using industry standard protocols.

RAID (Redundant Array of Independent Disks): a way for the same data to be stored in different places on many hard drives. By using this method, the data is stored redundantly and multiple hard drives will appear as a single drive to the operating system. RAID level 0 is known as striping, where data is striped (or overlapped) across multiple hard drives, but offers no fault-tolerance. RAID level 1 is known as mirroring, which stores the data within at least two hard drives, but does not stripe. RAID level 1 also allows for faster access time and fault-tolerance, since either hard drive can be read at the same time. RAID level 0+1 is both striping and mirroring, providing fault-tolerance, striping, and faster access all at the same time.

RAIDIOS: RAID I/O Steering (Intel)

RAM (Random Access Memory): technically refers to a type of memory where any byte can be accessed without touching the adjacent data and is often referred to the system's main memory. This memory is available to any program running on the computer.

**ROM (Read-Only Memory):** a storage chip which contains the BIOS; the basic instructions required to boot the computer and start up the operating system.

SDRAM (Synchronous Dynamic RAM): called as such because it can keep two sets of memory addresses open simultaneously. By transferring data alternately from one set of addresses and then the other, SDRAM cuts down on the delays associated with non-synchronous RAM, which must close one address bank before opening the next.

Serial port: called as such because it transmits the eight bits of a byte of data along one wire, and receives data on another single wire (that is, the data is transmitted in serial form, one bit after another).

SCSI Interrupt Steering Logic (SISL): Architecture that allows a RAID controller, such as AcceleRAID 150, 200 or 250, to implement RAID on a system board-embedded SCSI bus or a set of SCSI busses. SISL: SCSI Interrupt Steering Logic (LSI) (only on LSI SCSI boards)

Sleep/Suspend mode: in this mode, all devices except the CPU shut down.

**SDRAM (Static RAM):** unlike DRAM, this type of RAM does not need to be refreshed in order to prevent data loss. Thus, it is faster and more expensive.

**Standby mode:** in this mode, the video and hard drives shut down; all other devices continue to operate normally.

UltraDMA-33/66/100: a fast version of the old DMA channel. UltraDMA is also called UltraATA. Without a proper UltraDMA controller, your system cannot take advantage of higher data transfer rates of the new UltraDMA/UltraATA hard drives.

USB (Universal Serial Bus): a versatile port. This one port type can function as a serial, parallel, mouse, keyboard or joystick port. It is fast enough to support video transfer, and is capable of supporting up to 127 daisy-chained peripheral devices.

VGA (Video Graphics Array): the PC video display standard

V-SYNC: controls the vertical scanning properties of the monitor.

ZCR (Zero Channel RAID): PCI card that allows a RAID card to use the onboard SCSI chip, thus lowering cost of RAID solution

ZIF Socket (Zero Insertion Force socket): these sockets make it possible to insert CPUs without damaging the sensitive CPU pins. The CPU is lightly placed in an open ZIF socket, and a lever is pulled down. This shifts the processor over and down, guiding it into the board and locking it into place.

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# **Technical Support**

If a problem arises with your system, you should turn to your dealer for help first. Your system has most likely been configured by them, and they should have the best idea of what hardware and software your system contains. Furthermore, if you purchased your system from a dealer near you, you can bring your system to them to have it serviced instead of attempting to do so yourself (which can have expensive consequences).

If these options are not available for you then Tyan Computer Corporation can help. Besides designing innovative and quality products for over a decade, Tyan has continuously offered customers service beyond their expectations. Tyan's website (<a href="https://www.tvan.com">www.tvan.com</a> provides easy-to-access resources such as indepth Linux Online Support sections with downloadable Linux drivers a nd comprehensive compatibility reports for chassis, memory and much more. With all these convenient resources just a few keystrokes away, users can easily find the latest software and operating system components to keep their systems running as powerful and productive as possible. Tyan also ranks high for its commitment to fast and friendly customer support through email. By offering plenty of options for users, Tyan serves multiple market segments with the industry's most competitive services to support them.

"Tyan's tech support is some of the most impressive we've seen, with great response time and exceptional organization in general" - Anandtech.com

Please feel free to contact us directly for this service at techsupport@tyan.com

#### Help Resources:

- 1. See the beep codes section of this manual.
- 2. See the TYAN website for FAQ's, bulletins, driver updates,
- and other information: http://www.tyan.com
- 3. Contact your dealer for help BEFORE calling TYAN.
- 4. Check the TYAN user group: alt.comp.periphs.mainboard.TYAN

## **Returning Merchandise for Service**

During the warranty period, contact your distributor or system vendor FIRST for any product problems. This warranty only covers normal customer use and does not cover damages incurred during shipping or failure d ue to the alteration, misuse, abuse, or improper maintenance of products.

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NOTE: A receipt or copy of your invoice marked with the date of purchase is required before any warranty service can be rendered. You may obtain service by calling the manufacturer for a Return Merchandise Authorization (RMA) number. The RMA number should be prominently displayed on the outside of the shipping carton and the package should be mailed prepaid. TYAN will pay to have the board shipped back to you.



## Notice for the USA

Compliance Information Statement (Declaration of Conformity Procedure) DoC FCC Part 15: This device complies with part 15 of the FCC Rules

Operation is subject to the following conditions:

This device may not cause harmful interference, and This device must accept any interference received including interference that may cause undesired operation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try one or more of the following measures:

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and the receiver. Plug the equipment into an outlet on a circuit different from that of the receiver. Consult the dealer on an experienced radio/television technician for help.

#### Notice for Canada

This apparatus complies with the Class B limits for radio interference as specified in the Canadian Department of Communications Radio Interference Regulations. (Cet appareil est conforme aux norms de Classe B d'interference radio tel que specifie par le Ministere Canadien des Communications dans les reglements d'intetference radio.)



Notice for Europe (CE Mark)
This product is in conformity with the Council Directive
89/336/EEC, 92/31/EEC (EMC).

CAUTION: Lithium battery included with this board. Do not puncture, mutilate, or dispose of battery in fire. Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by manufacturer. Dispose of used battery according to manufacturer instructions and in accordance with your local regulations.

Document #: D1731-100

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